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MONOLITHIC GaAs DUAL-GATE FET PHASE SHIFTER

RCA Laboratories
Princeton, New Jersey 08540

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Progress

1. The photomask of a 0 to 90° monolithic GaAs dual-gate FET phase shifter has been procured, and we are in the process of fabricating the phase shifter.

2. We have designed and fabricated a 50-Ω, 4-line interdigitated coupler. Also, we have designed and fabricated a 25-Ω, 6-line inter-

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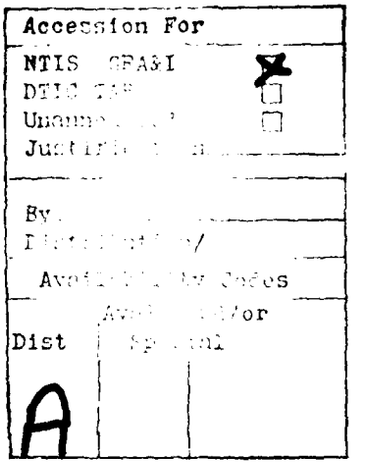
digitated coupler. The performance of both couplers agrees quite quite well with the theoretical results.

Technical Problems

There was no major problem during this period.

PREFACE

This Tri-annual report describes the work performed under Contract No. N00014-79-C-0568, 1 May 1981 to 31 August 1981, in the Microwave Technology Center, F. Sterzer, Director. H. C. Huang is the project supervisor, and M. Kumar is the project scientist.



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I. OBJECTIVE

The objective of this four-year program (Sept. 1, 1979 to Aug. 31, 1983) is to develop a monolithic GaAs dual-gate FET phase shifter, operating over the 4- to 8-GHz frequency band and capable of a continuously programmable phase shift from 0° through N times 360° where N is an integer. The phase shift is to be controllable to within ±3°. This phase shifter will be capable of delivering an output power up to 0 dBm with an input and output VSWR of less than 1.5:1.

II. PROGRESS

In the last tri-annual report, for the period 1 January 1981 to 30 April 1981, we reported the development of "via" hole techniques and the development of a four-way planar combiner. We also reported the progress made in the development of a 90° monolithic GaAs dual-gate FET phase shifter. During this reporting period, we have developed the 50-Ω, 4-line and 250-Ω, 6-line interdigitated 90° couplers on GaAs semi-insulating substrates. We are also in the process of fabricating a 90° monolithic phase shifter.

A. Development of a 50-Ω, 4-Line Interdigitated Coupler

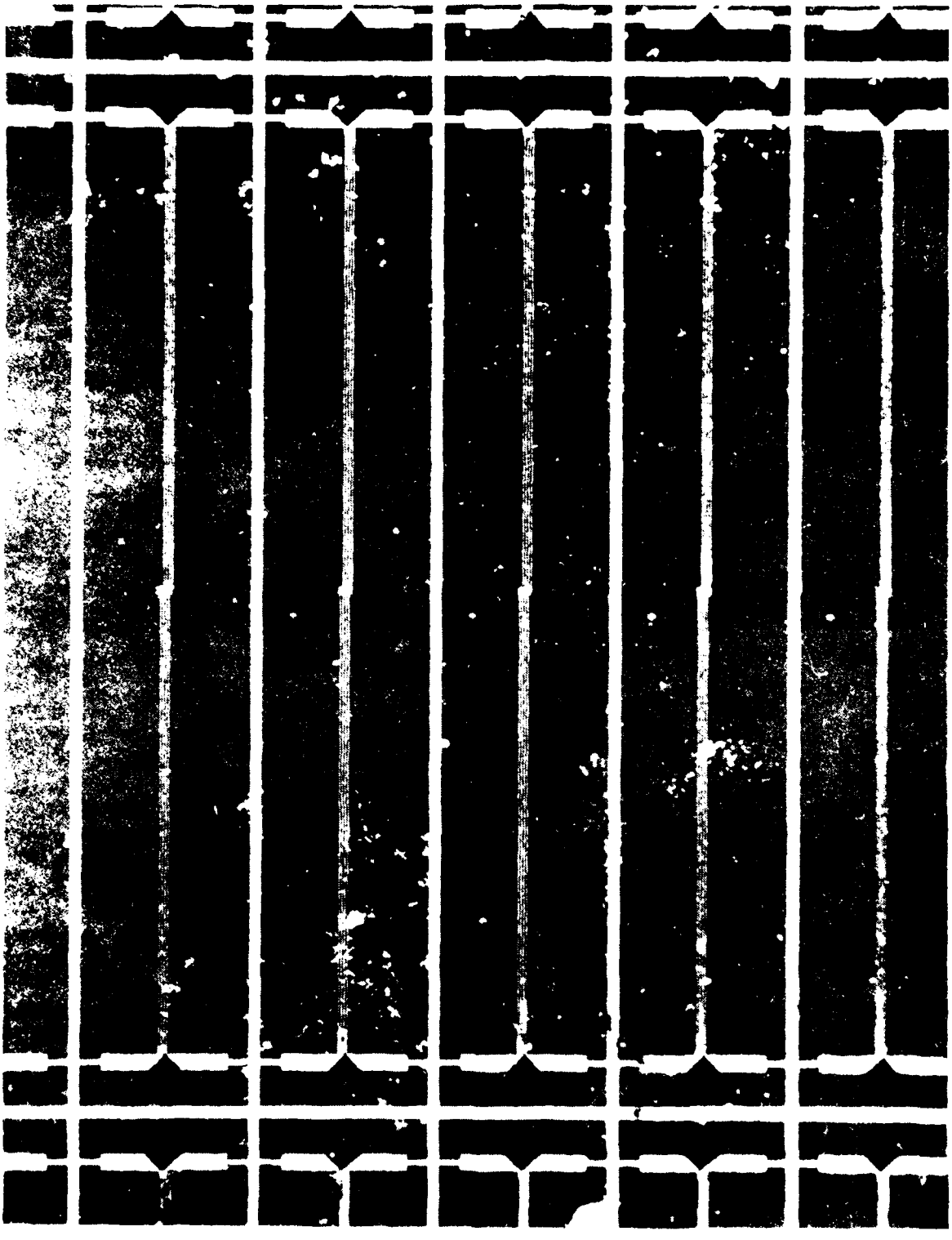
We have designed, fabricated, and tested a 50-Ω, 4-line interdigitated coupler which is a key component of the 90° phase shifter. The coupler was designed using the CAD program developed at the RCA Laboratories. The width and spacing of the interdigitated conductors are 6.5 μm and 7.0 μm, respectively. The length of the coupler is 4.39 mm. The thickness of the GaAs substrate is 0.1 mm. This coupler was designed for operation in the C band (4 to 8 GHz). The coupler was first fabricated on a 0.38-mm (15-mil) thick SI GaAs substrate using the lift-off technique. Airbridge interconnections were used to minimize the crossover capacitance. The wafer was later lapped to a thickness of 0.1 mm and was metallized on the backside to form a ground plane. To facilitate testing of the coupler, 50-Ω lines on 10-mil-thick Al_2O_3 substrate were used to connect the coupler ports to the SMA connectors. The losses of the Al_2O_3 test fixture were calibrated and subtracted from the measurement results. The results presented here are the true results of the coupler, excluding the losses of the test fixture.

Figure 1 shows the photograph of the coupler, and Fig. 2 shows the SEM of the airbridge connection of the interdigitated conductors of the coupler. The calculated and measured results of the coupling are presented in Fig. 3. The measured results are in close agreement with the calculated results. The coupler performed well over the 4- to 8-GHz band. The variation of insertion loss and phase difference between two output ports is presented in Fig. 4. The coupler has an average loss of about 0.5 dB over the 4- to 8-GHz band. The phase differences between the two output ports are $90° \pm 2°$. The isolation and VSWR at any port of the coupler are better than 18 dB and 1.4, respectively, over the entire 4- to 8-GHz band.

B. Development of a 25-Ω, 6-Line 90° Interdigitated Coupler

A monolithic interdigitated 90° coupler is an important passive component of the phase shifter as well as for microwave monolithic integrated circuit (MMIC) applications such as balanced amplifiers, mixers, discriminators, etc. The input and output impedances of a GaAs FET are on the order of a few ohms. In a conventional approach in MMICs, these input and output impedances have to be matched to 50 Ω. To overcome such a large mismatch from a few to 50 Ω, multisection matching networks have to be used. This leads to high loss in the matching networks and a relatively large matching network which consumes a large area of GaAs real estate. This problem becomes more serious when high frequency, high power, and multi-stages are required. Use of a lower than 50-Ω system (such as a coupler having a 25-Ω impedance, for example) will result in matching circuits with fewer matching elements, producing a saving in the GaAs substrate area and a reduced loss in the matching circuits.

In view of the above observations, we have developed a 25-Ω, 6-line monolithic interdigitated 90° coupler on a 0.1-mm-thick GaAs SI substrate. The width and spacing of the interdigitated conductors are 19.0 μm and 11.0 μm, respectively. Figure 5 shows a photograph of the coupler, and Fig. 6 shows the SEM of the airbridge connection of the interdigitated conductors of the coupler. The results on coupling are presented in Fig. 7. The measured coupling agrees well with the theoretical calculation which is also included in Fig. 7. Also presented in Fig. 7 is variation of insertion loss with frequency. The average insertion loss of the coupler is 0.3 dB over the 4- to 8-GHz frequency band.



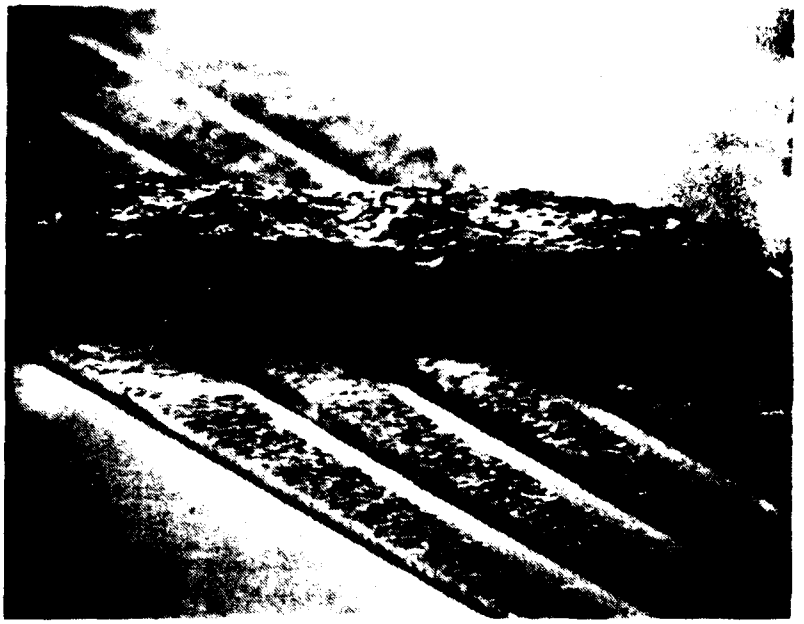


Figure 2. SEM of the airbridge connection of the 50-Ω, 4-line coupler.

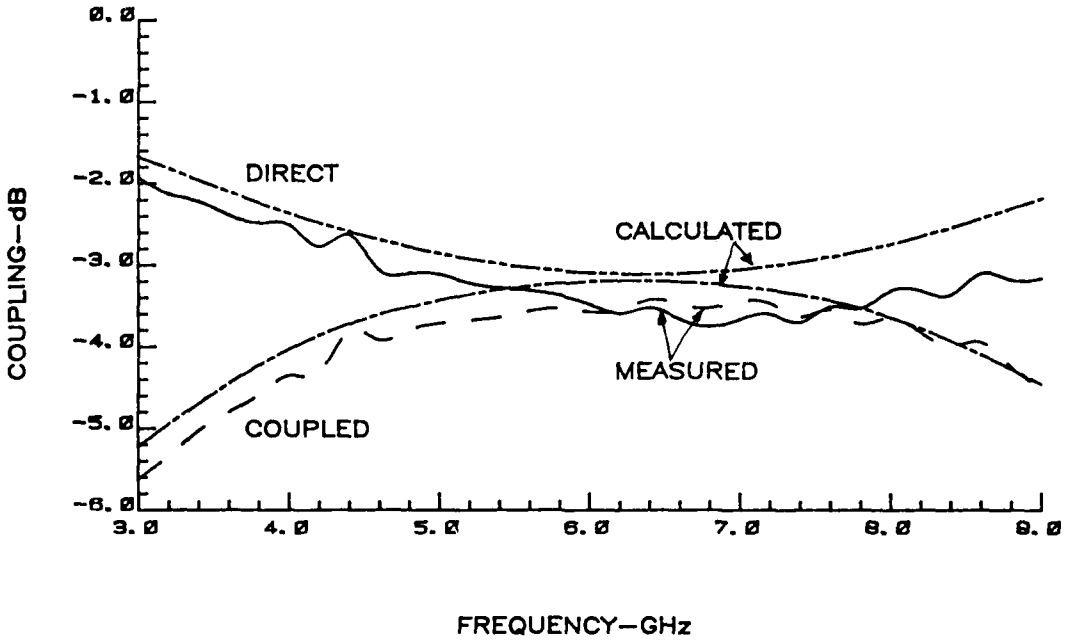


Figure 3. Coupling variation with frequency of a 50-Ω, 4-line coupler.

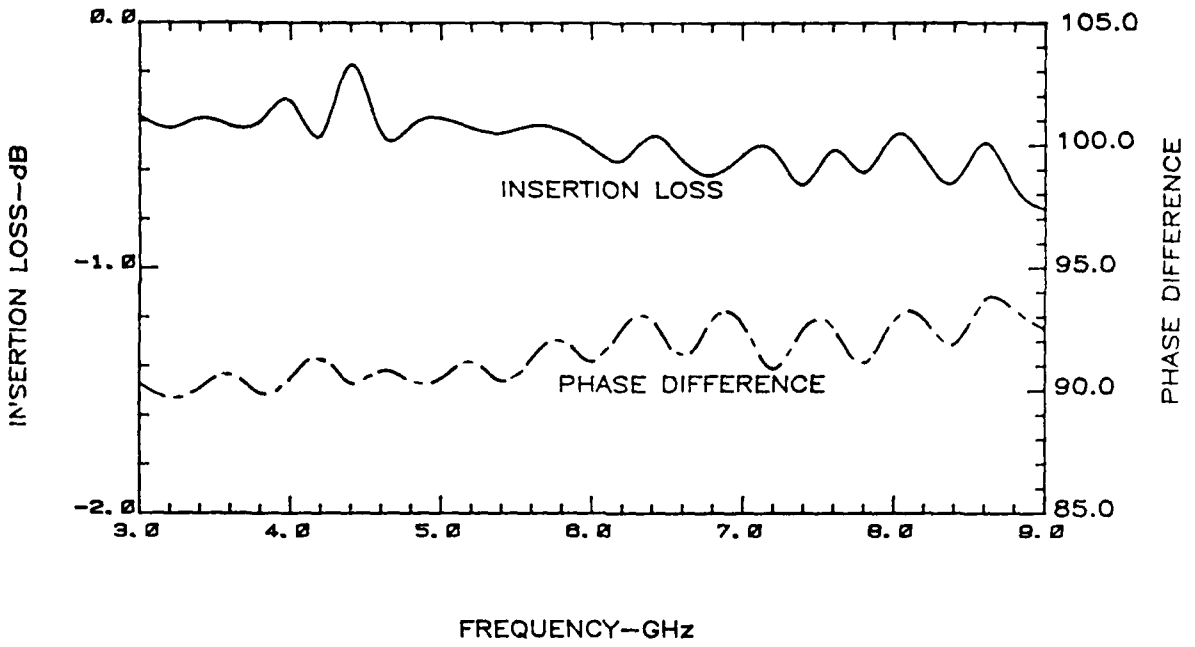


Figure 4. Variation of insertion loss and phase difference with frequency between two output ports of 50-Ω, 4-line coupler.

The isolation between the two output ports is better than 18 dB, and the phase imbalance is 90°±2°.

The coupler was tested on a 50-Ω system, and a 25- to 50-Ω λ/16, four-section transformer on a 10-mil Al_2O_3 substrate was used to connect the coupler ports to the 50-Ω system. The fixture and transformer losses were subtracted from the measured results. The results presented in Figs. 6 and 7 do not include fixture losses.

The insertion loss of the 6-line coupler is 0.3 dB across the 4- to 8-GHz band as compared to 0.5 dB for the 4-line coupler. The 25-Ω, 6-line coupler has two advantages over the 50-Ω, 4-line coupler; namely, better matching to FET and larger interdigitated conductor width resulting in lower loss.

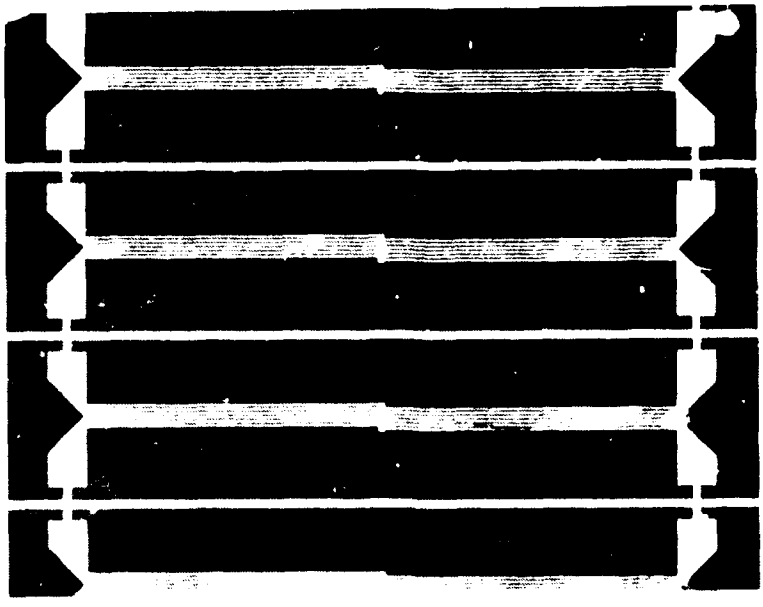


Figure 5. Photograph of the 25-Ω, 6-line coupler.

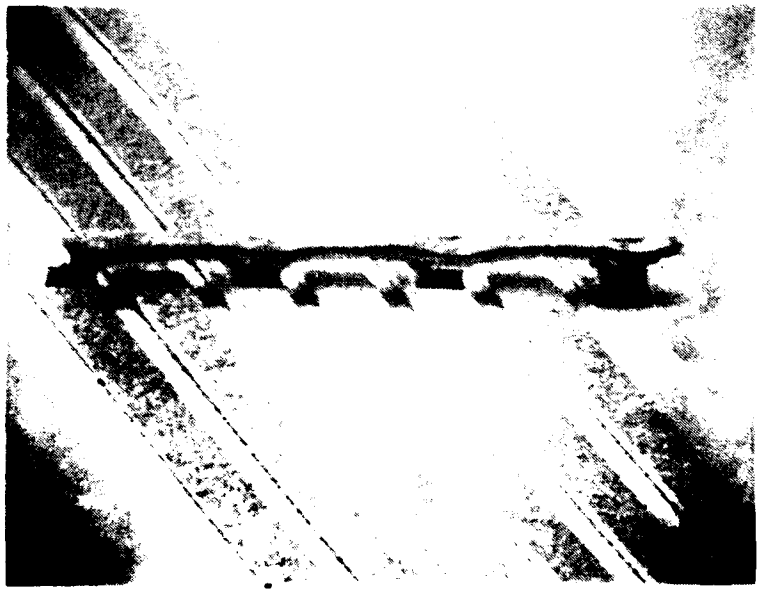


Figure 6. SEM of the airbridge connection of the 25-Ω, 6-line coupler.

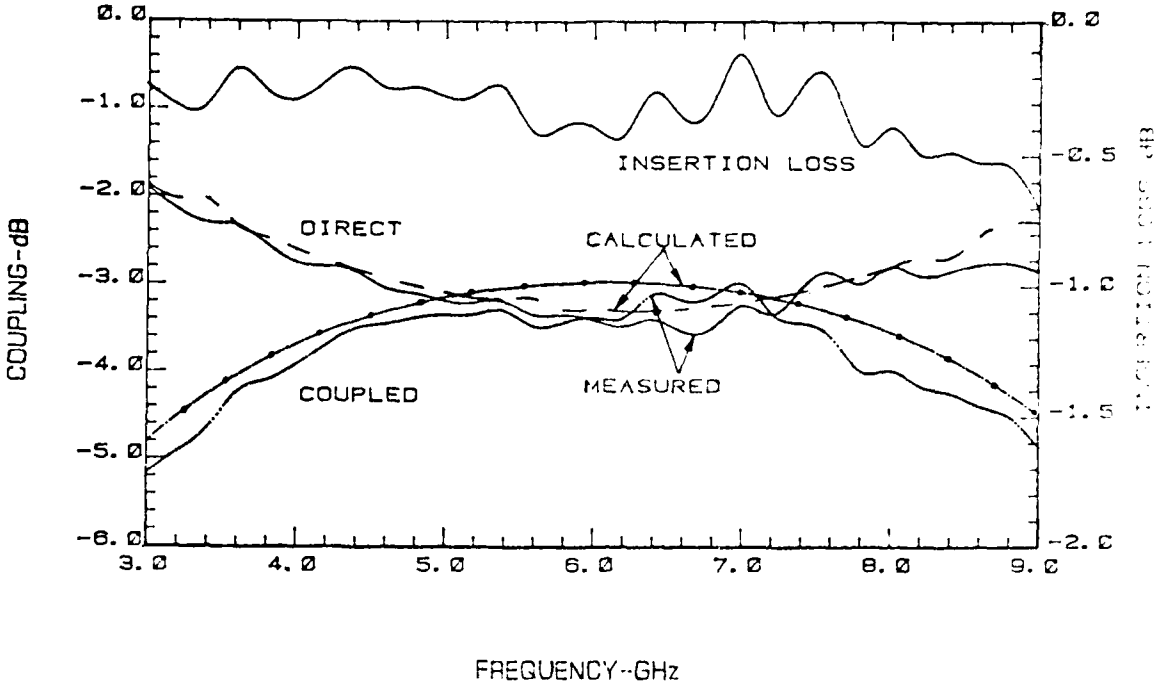


Figure 7. Coupling and insertion loss variation with frequency of a 25-Ω interdigitated coupler.

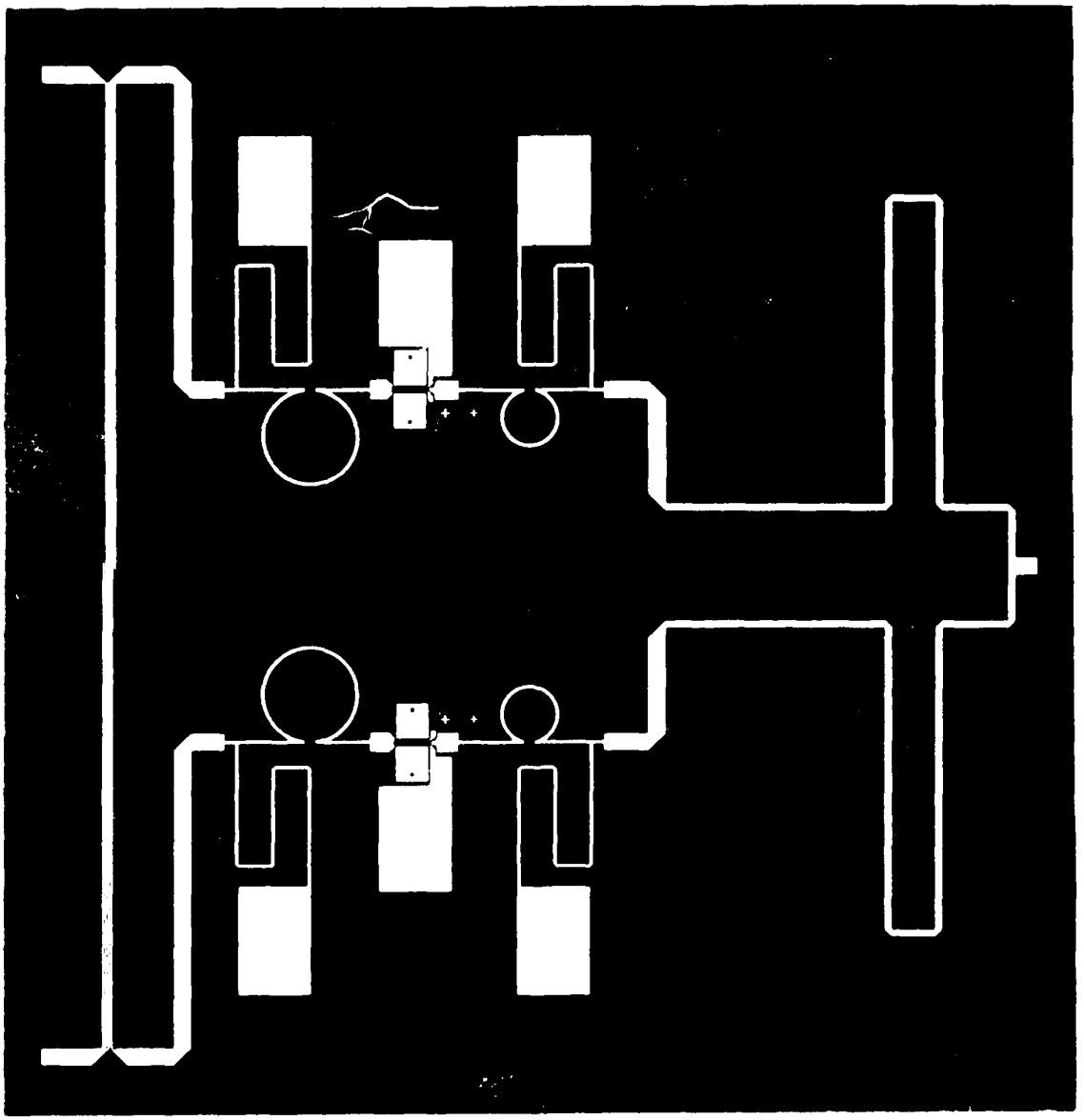
C. Development of Monolithic 90° Phase Shifter

The photomasks for the 90° monolithic dual-gate FET phase shifter have been procured. We are in the process of fabricating the phase shifter. This phase shifter chip consists of a 90°, interdigitated coupler, two dual-gate FET amplifiers, an in-phase power combiner, and bypass capacitors. The design of the phase shifter is shown in Fig. 8.

The processing of the phase shifter includes the fabrication of:

(a) capacitors using sputter-deposited Si_3N_4 (2000 Å) as the dielectric,

(b) resistors using Ti,



Currently, we are experiencing some difficulty in defining the gates using the new masks which we received from Photronics Labs.* We are trying to identify the problem connected with the mask with the help of the manufacturer and are hopeful that the problem will be resolved shortly.

III. PUBLICATIONS

The following papers have been published during the past year:

1. M. Kumar, G. Taylor, and H. Huang, "Design consideration for monolithic GaAs FET amplifier," presented at 1980 GaAs IC symposium, paper #23, November 4-6, 1981, Las Vegas, Nevada.
2. M. Kumar, G. Taylor, and H. Huang, "Monolithic dual-gate GaAs FET amplifier," IEEE Trans. Electron Devices ED-28, 197 (1981).
3. M. Kumar, R. J. Menna, and H. C. Huang, "Broadband dual-gate continuously variable phase shifter," 1981 IEEE MTT-S International Microwave Symposium Digest, pp. 431-433, June 15-17, 1981, Los Angeles, California.

Copies of these papers are included as Appendices A, B, and C.

* Photronics Labs, Inc., Danbury, CT

APPENDIX A

DESIGN CONSIDERATIONS FOR MONOLITHIC GaAs FET AMPLIFIER*

M. Kumar, G. Taylor and H. Huang, RCA Laboratories,
David Sarnoff Research Center, Princeton, N.J. 08540;
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One of the major concerns in the development of monolithic microwave integrated circuits is the long iteration time required before the final design is completed. Each iteration is time-consuming because it involves redesign of the mask pattern as well as fabrication and testing. This paper presents a systematic analytical method for designing broadband impedance matching circuits for monolithic FET amplifiers. This design method leads to an optimal circuit topology with least iteration so that the amplifier performance is least sensitive to variations in the circuit and device parameters.

The design method begins with sensitivity analysis of four different possible types of input and output matching networks, respectively. Each matching network consists of two lumped circuit elements in the configuration of shunt inductance-series inductance, series L-shunt C, series L-shunt L, and shunt L-series C. This same sensitivity analysis is then repeated for the output matching network. After a least sensitive circuit is obtained, additional circuit elements can be added to improve the gain flatness over the desired frequency band using a computer-aided design method.

The design method is explained with an example using the S-parameters of a NEC dual-gate FET. The sensitivity analysis for this case indicates that the shunt L-series L configuration is optimal for the input and the series L-shunt C configuration for the output. With this circuit topology, a variation of $\pm$10% in circuit element value leads to less than 0.3 dB change in gain across the 4-8 GHz octave bandwidth. While in a non-optimal circuit topology, a $\pm$10% variation in circuit element value can lead to as much as 1.5 dB gain change over the same band. Furthermore, our sensitivity analysis indicates that two circuit elements for the input and output circuit, respectively, are enough for the determination of optimal circuit topology. Additional circuit elements, while improving the gain flatness, contribute only a secondary effect to the sensitivity of the topology.

This method has been applied to the design of a monolithic dual-gate FET amplifier with lumped-circuit matching networks. Without any iteration or external tuning, a gain of 5 dB has been achieved from 5.5 to 8 GHz. We believe that this systematic design approach is the first time reported for the design of monolithic linear GaAs FETs. The design method can be applied equally well to monolithic low-noise FET amplifiers, power FET amplifiers, dual-gate FET amplifiers, and FET oscillators. Details in the sensitivity analysis as well as monolithic dual-gate FET fabrication and performance will be presented.

*This work was supported by the Office of Naval Research, Arlington, Virginia, under Contract No. N00014-79-C-0568.

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. ED 28, NO. 2, FEBRUARY 1981

Monolithic Dual-Gate GaAs FET Amplifier

MAHESH KUMAR, MEMBER, IEEE, GORDON C. TAYLOR, MEMBER, IEEE, AND HO-CHUNG HUANG, SENIOR MEMBER, IEEE

Abstract—**This paper presents the design, fabrication, and performance of a broad-band monolithic dual-gate GaAs FET amplifier. The amplifier has a gain of 3.5–5 dB over the 4.5- to 8-GHz band.**

I. Introduction

IN RECENT YEARS, the dual-gate FET has attracted considerable attention because of its versatility as a microwave, multifunction device. It can be used in switches, mixers, multipliers, up-converters, discriminators, phase shifters, and variable-gain amplifiers. The design of a monolithic dual-gate FET C-band amplifier using a totally lumped component approach offers the opportunity of miniaturization for low-noise or broad-band applications.

One of the major concerns in the development of monolithic microwave integrated circuits is the long iteration time required before the final design is completed. There are a number of variations that cannot be predicted with sufficient accuracy for the normal circuit design technique to perform satisfactorily. These variations can result from the lumped circuit element values, from the material characteristics, and from the physical dimensions. With these considerations, we have designed a monolithic dual-gate FET amplifier with an attempt to minimize the performance sensitivity to the circuit variations. The computer-aided design technique is used to predict the performance of the amplifier. An optional design approach is chosen by performing the sensitivity analysis of the final performance of the amplifier for the variation in each matching element. The amplifier is fabricated using the liftoff technique. The amplifier has a gain of 3.5–5 dB over the C-band. The design and fabrication details are presented.

II. Design, Fabrication, and Performance

A monolithic dual-gate FET amplifier is designed using lumped circuit element approaches over 4–8 GHz. The computer-aided design technique is used to obtain the optimal circuit approach and to perform the sensitivity analysis of each matching element. Each element is varied by ±10 percent of its nominal value and its effect on gain of the amplifier is analyzed. The circuit diagram of the amplifier is shown in Fig. 1. This circuit approach (Fig. 1) showed a 0.5-dB gain variation over the band with ±10-percent variations in all the element values. The photograph of the amplifier is shown in Fig. 2.

Manuscript recieved August 8, 1980; revised September 23, 1980. This work was supported by the Office of Naval Research, Arlington, VA, under Contract N00014-79-C-0565, monitored by M. N. Yoder.

The authors are with RCA Laboratories, David Sarnoff Research Center, Princeton, NJ 08540.

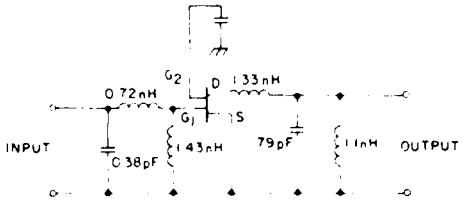

Fig. 1. Circuit diagram of GaAs monolithic dual-gate FET amplifier.

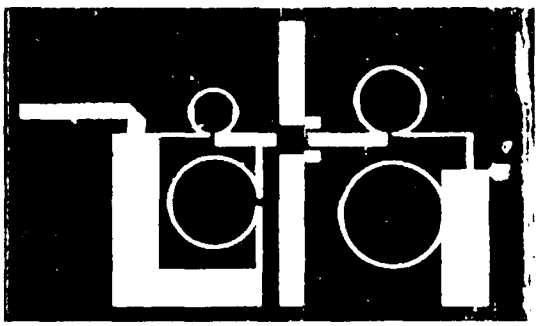

Fig. 2. Photograph of the GaAs monolithic FET amplifier.

The fabrication of monolithic dual-gate FET amplifiers begins with an n^+-n-semi-insulating GaAs wafer. The nominal carrier density of the active layer is 1×10^{17} cm^{-3} and that of the n^+ layer is 1×10^{18} cm^{-3}. Each epitaxial layer is nominally 0.5 μm thick. A variation of the anodic thinning process [1] is used to thin the active channel areas to the "pinchoff" thickness while leaving n^+ material in the source and drain regions. Individual devices are then isolated using a citric acid etchant [2] to produce the mesa region. Ohmic contacts are produced by the liftoff of AuGe/Ni (1500 Å/500 Å) and sintering at 450°C for 60 s.

Prior to defining the gates in photoresist, the device channels are chemically etched to adjust the saturation current and a 0.1-μm-thick layer of titanium is deposited uniformly across the wafer. This titanium layer serves to improve the adhesion of the gate metallization and as a conduction path for Au plating. The nominal 1.5-μm-long gates and matching element components are next defined in photoresist for the liftoff of Ti/Pt/Au metallization approximately 0.5 μm thick. Liftoff is again used to increase the metal thickness on the ohmic contacts by depositing Ti/Pt/Au. After liftoff, the matching elements are redefined in thick photoresist (8–10 μm) and plated with 6–7 μm of gold. After careful solvent cleaning, the tita-

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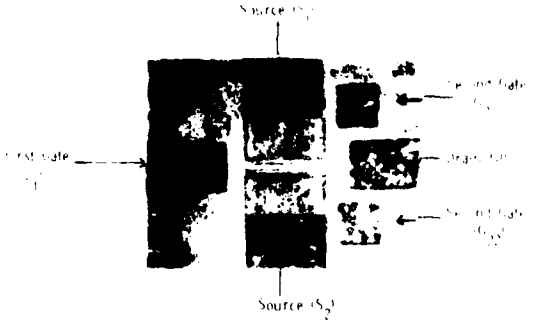

Fig. 3. Photograph of the GaAs dual-gate FET.

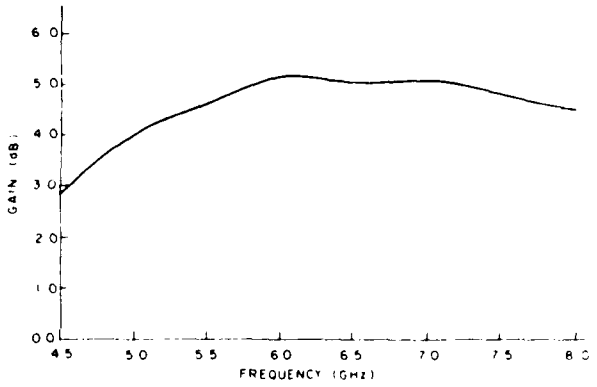

Fig. 4. Gain as a function of frequency of the GaAs monolithic dual-gate FET amplifier.

mum layer is chemically etched away with an etchant containing HF, HNO_3, and H_2O [3]. Fig. 2 shows the monolithic amplifier chip. A photograph of the dual-gate FET is shown in Fig. 3. The unit gate width is 150 μm. The length of the first and second gates is 1.5 μm. The separation between the first and the second gate is 3 μm and the source to drain spacing is 9 μm.

Fig. 4 shows the gain of the amplifier as a function of frequency over 4–8-GHz band. The preliminary results show that a gain of 3.5–5 dB is obtained over the band with the second gate grounded. This gain is achieved without any trimming of the circuit elements.

III. Conclusion

A dual-gate monolithic GaAs FET amplifier is fabricated and initial results show a gain of 3.5–5 dB over the 4.5–8-GHz band. The monolithic dual-gate FET amplifier was designed for use in a phase shifter, but such monolithic amplifiers offer a wide potential as multifunction devices.

Acknowledgment

The authors wish to thank P. Pelka and R. Menna for their help in assembling and testing of the amplifier.

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[1] D. L. Rode, B. Schwartz, and J. V. DiLorenzo, "Electrolytic etching and electron mobility of GaAs for FETs," *Solid-State Electron.*, vol. 17, pp. 1119–1123, 1974.

[2] M. Otsubo, J. Oda, H. Kumabe, and H. Miki, "Preferential etching of GaAs through photoresist masks," *J. Electrochem. Soc. Solid State Sci. Technol.*, vol. 123, no. 5, May 1976.

[3] F. Murai, H. Kurono, and H. Kodera, "Intentional side etching to achieve low noise GaAs FET," *Electron. Lett.*, vol. 13, no. 11, May 26, 1977.

APPENDIX C

BROADBAND DUAL-GATE FET CONTINUOUSLY VARIABLE PHASE SHIFTER*

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RCA Laboratories
Princeton, NJ 08540

ABSTRACT

This paper describes a broadband, GaAs dual-gate FET phase shifter capable of continuous phase shift from 0° - 360° over the 4-8 GHz band. Although the present unit is in discreet form, it is designed to be compatible with monolithic fabrication technology.

Introduction

In the past, ferrite phase shifters have been used in the phased array radar systems. Recently PIN diode phase shifters are being considered because of their lighter weight, higher speed and transmission reciprocity as compared to the ferrites.[1,2] The ferrite and PIN diode phase shifters, however, still suffer from a relatively high signal loss and relatively slow response time. The recent interest in fully-active phased array radars as well as progress in the monolithic GaAs integrated circuits has opened the possibility of realizing active phase shifting subassemblies based upon GaAs field-effect transistors (FETs).

The dual-gate FET has been used in many applications such as variable-gain amplifiers[3], power limiters, discriminators and mixers[4], etc. A single-frequency, dual-gate FET phase shifter has been reported.[5,6] The phase shift is obtained by changing the dc voltage applied to the control gate of the FET, and a linear phase shift of about 100° has been obtained over a narrow frequency band. Recently, a narrow-band phase shifter using dual-gate GaAs FETs has also been reported.[7] The phase shift in this case is obtained by complex vector addition of two orthogonal vectors. This circuit operates over a bandwidth of 1 GHz in the X-band. In this configuration, four variable gain amplifiers are required to achieve a 360° phase shift.

This paper presents the design and development of a broadband, dual-gate FET phase shifter operating over the 4-8 GHz band, capable of a continuous phase shift from zero through N times 360° where N is an integer. The phase shift is obtained by the vector sum of four orthogonal signals whose amplitudes can be varied over a wide dynamic range. Four dual-gate FET amplifiers are used as variable gain amplifiers for the amplitude control. This phase shifter has been realized on a microstrip circuit, and is compatible to monolithic integration on a GaAs substrate. The work on developing the monolithic phase shifter is in progress.[8]

The phase shifter reported here offers the advantages of low loss (3.5 dB maximum), fast response time of less than 100 ns, and octave bandwidth of 360° continuous phase shift. It is suitable for applications in serrodyning, beam steering, and biphase modulation for secure communication or coding.

I. Principle of Phase Shifter

Fig. 1 illustrates the schematic of a continuously-variable 0° to 360° phase shifter. The 360° phase shift is achieved by the sum of 4 quadrature vectors A∠0°, B∠90°, C∠180° and D∠270° with properly-controlled amplitudes of A, B, C and D. Those 4 quadrature vectors can be realized by a 180° power divider, two 90° hybrids, four dual-gate FET amplifiers and an in-phase, four-way power combiner as shown in Fig. 1. The incoming signal is first divided into two signals which are equal in amplitude but 180° apart in phase. Then each signal is further divided into two signals through a 90° hybrid, resulting in four signals of equal amplitude and having

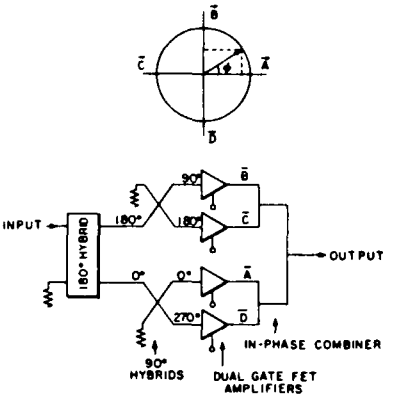

FIGURE 1: SCHEMATIC OF A 360° GaAs DUAL-GATE FET PHASE SHIFTER.

phases of 0°, 90°, 180° and 270°. Each signal is then amplified through a dual-gate FET amplifier, and the four outputs are then combined through a four-way, in-phase combiner to obtain a phase-controlled output. Fig. 1 illustrates the four quadrants of 360° phase shift which are obtained using a combination of two vectors at a time. Each dual-gate FET serves as an amplifier-switch which can control the amplitudes of the vectors $\vec{A}$, $\vec{B}$, $\vec{C}$ and $\vec{D}$. As an example, when $\vec{C}$ and $\vec{D}$ are switched off, $\vec{A}$ and $\vec{B}$ are switched on, an output signal with about 30° phase advance relative to the input signal is obtained [Fig. 1]. By changing the second gate bias voltages of amplifiers A and B (when C and D are switched off), the total 0° to 90° phase shift can be obtained. Thus by controlling the bias voltages of two amplifiers at one time, while the other two are switched off, a total of 360° continuous phase shift is obtained.

II. Design, Fabrication and Performance

The design of the phase shifter involves the design of the following components: 180° hybrid, 90° hybrid, four-way combiner and dual-gate FET amplifier. A 180° planar hybrid is realized using a 90° interdigitated hybrid and a 0-dB tandem coupler. The schematic of the 180° hybrid is shown in Fig. 2. It is a four-port device. Ports 1 and 2 are the input ports and Ports 3 and 4 are the output ports. When the signal is fed to Port

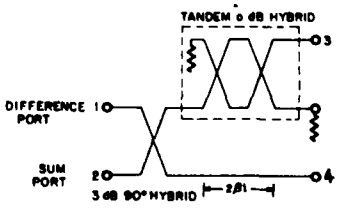

FIGURE 2: SCHEMATIC OF A 180° HYBRID.

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1 and Port 2 is match terminated, the signals appearing at Port 3 and Port 4 are both 3 dB below the input signal and have a phase difference of 180°. This hybrid has 3 GHz bandwidth over the 4-8 GHz band, and a phase unbalance of ± 7°.

The design of the 90° hybrid (interdigitated) and a four-way Wilkinson power combiner is standard and is not discussed here. The dual-gate FET amplifier design is done using CAD techniques.[3] Fig. 3 shows the variation of gain with frequency for different second gate bias voltages. The gain of the amplifier can be varied from 10 dB to -30 dB (cut-off) by changing the second gate (control gate) bias voltage. The photograph of the

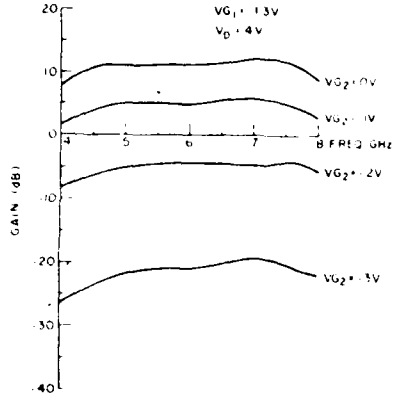

FIGURE 3: VARIATION OF GAIN VS BIAS VOLTAGES (V_{G2}) OF A DUAL-GATE FET AMPLIFIER.

360° phase shifter is shown in Fig. 4. All the passive circuit components such as the 90° and 180° hybrids, Wilkinson four-way power combiner and dc bias circuits of the dual-gate FETs are designed in the planar form so that the complete phase shifter can readily be integrated on a monolithic GaAs chip. Fig. 5 shows the variation of phase shift with control voltages (the second gate bias voltages). The 0° to 360° continuous phase shift is obtained by changing the second gate bias voltages of the dual-gate FET amplifiers in a systematic

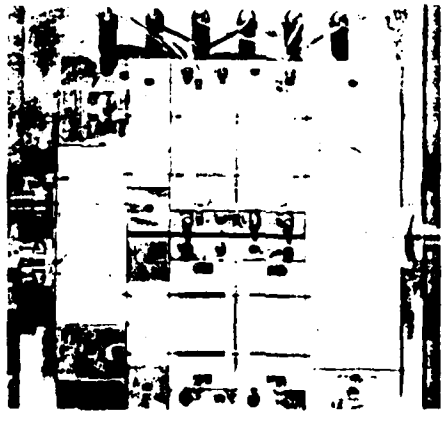

FIGURE 4: PHOTOGRAPH OF THE 360° PHASE SHIFTER.

manner. Referring to Fig. 5, there are four sections which divide the total phase shift of 360° by four dotted, vertical lines. Each section represents the phase control of one quadrant. In each quadrant, the control voltages of two dual-gate FET amplifiers are varied, while the remaining two amplifiers are switched

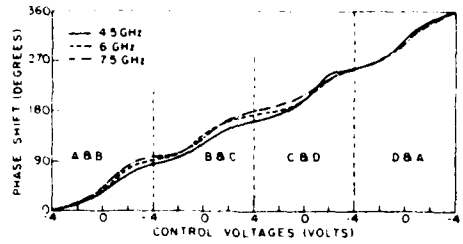

FIGURE 5: VARIATION OF PHASE WITH CONTROL VOLTAGES OF 360° PHASE SHIFTER.

off by applying -4V[3] to their second gates. For example, in the first quadrant, the V_{G2}'s for A and B are varied while the V_{G2}'s for C and D are kept at -4 volts for switched-off conditions. Now to get a 90° phase shift, amplifier A is kept under the on condition ($V_{G2}(A)$ = 0 volts) and $V_{G2}(B)$ for amplifier B is varied from -4 volts to 0 volts which gives approximately the 45° phase shift (Fig. 4). Next, amplifier B is switched on ($V_{G2}(B)$ = 0 volts) and the $V_{G2}(A)$ for amplifier A is varied from 0 to -4 volts which gives approximately from 45° to 90° phase shift. Thus controlling the two second gate bias voltages of two amplifiers, a 90° phase shift is obtained. This process is repeated with other combinations of two orthogonal vectors to obtain the entire 0° to 360° phase shift.

The variation of amplitude with phase is presented in Fig. 6. The gain of the phase shifter is plotted as a function of phase for different frequencies. The maximum variation of gain is ±3 dB for a 360° phase shift. As explained earlier, the phase shift at 0°, 90°, 180° and 270° is obtained by switching three amplifiers off while leaving only one amplifier on; this gives a variation of 5 dB in amplitude because of the four-way power combination characteristics.[9,10] It is possible to achieve a constant output power for any given phase by properly programming the control gate bias voltages.

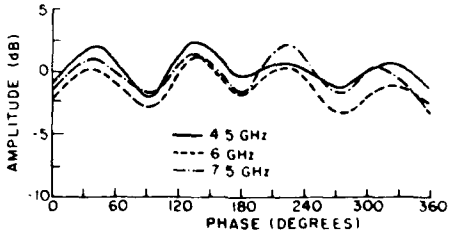

FIGURE 6: VARIATION OF AMPLITUDE WITH PHASE OF 360° PHASE SHIFTER.

III. Conclusions

A broadband active phase shifter has been presented, operating over the 4-8 GHz band. The 360° continuous phase shift is obtained with minimal loss. The phase shifter design presented here is compatible to monolithic integration on GaAs substrates. Work on the development of a monolithic phase shifter is in progress. This phase shifter has several advantages over other kinds of phase shifters - in light weight, fast response, low loss, and octave bandwidth capability.

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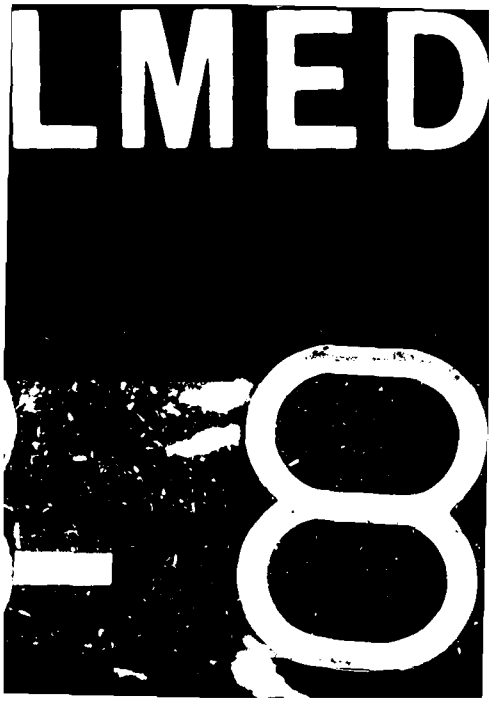
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